removing the second silica layer from the etching area using the mask by dry etching; and

removing the etch stop layer by wet etching.

REMARKS

Claims 2 and 11 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Claims 1, 3, 6, 10, 12, 15 and 17 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S Patent No. 6,306,706 (hereinafter "Chan"). Claims 4, 7, 9, 13, 16 and 18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chan in view of U.S. Patent No. 5,284,549 (hereinafter "Barnes"). Claims 19 and 20 have been objected to as having no patentable weight. Independent claims 1 and 10 have been amended to clarify the claimed invention.

Claims 2, 4, 11, 13 and 18 have been canceled and thereby obviate the objections and rejections raised by the Examiner. Further, Applicant respectfully submits that claims 19 and 20 are proper Product-by-Process claims; see MPEP 706.03(e), which states: "An article may be claimed by a process of making it..." If the Examiner objects to these claims, Applicants request clarification of such an objection and to the above comment of the present Office Action.

On the merits, Applicant respectfully submits that the pending claims, as amended, are patentable for at least the following reasons.

Amended independent claim 1 is directed to a silica microstructure fabrication method comprising the steps of depositing an etch stop layer formed of one of gold,

platinum, and alumina on an etching area of a portion of a first silica layer formed on a semiconductor substrate, forming a second silica layer on the surfaces of the etch stop layer and the first silica layer, forming a mask patterned according to the shape of the etching area on the surface of the second silica layer, removing the second silica layer from the etching area using the mask by dry etching; and removing the etch stop layer by wet etching. Support for the amendment can be found at least in page 6, lines 7-12. Amended independent claim 10 recites similar limitations.

In addressing the presently recited "depositing an etch stop layer" in the above rejection, the poly2 layer (Figure 5c) of Chan is being relied on. However, in column 2, lines 25-29, Chan discloses that the core and periphery regions of a flash memory are etched separately after the deposition of poly2 layer in order to reduce the occurrence of residue materials known as stringers at the core/periphery interface. The poly layers in Chan (poly1 and poly2) are polysilicon, which are used to form transistors and connections therebetween, see col. 1 lines15-20 and lines 45-60 of Chan.

In contrast, the present invention discloses a method of stopping etching process at a desired position by providing an etch stop layer formed of one of gold, platinum, and alumina. Accordingly, applicants have found no indication in Chan that even shows any recognition of the advantages or the desirability of the limitations recited in claim 1.

Furthermore, Applicants can find nothing in Chan that teaches an etch stop layer having a high etch selectivity with respect to silica, such as gold, platinum, and alumina, as specifically recited in claim 1, see specification on page 6, lines 6-12.

Based on the above disclosure, it is respectfully submitted that the presently recited "depositing an etch stop layer formed of one of gold, platinum, and alumina on an etching

area of a portion of a first silica layer formed on a semiconductor substrate" is not anticipated by Chan.

Further, applicant respectfully submits that reliance of Chan in rejecting pending claims is improper. Chan, as read by applicant, relates to a method for fabricating **silicon microstructure,** while the present invention relates to a method of fabricating **silica microstructures**. In particular, the present invention discloses a silica micro-structure comprising a planar lightwave circuit (PLC) made of silica for reducing optical loss when connecting the PLC with an optical fiber made of silica. It is respectfully submitted that the silicon micro-structure of the Chan would be difficult to be applied to the PLC as silicon may cause a large optical loss. As such, there is no basis that technical feature applied to the silicon micro-structure of the Chan can be applied to a silica micro-structure of the present invention.

It is well settled that a reference that does not teach or suggest all of the features of a claimed invention cannot anticipate that invention. Since Chan does not teach or suggest all of the features of amended independent claims 1 and 10, as recited above, applicant respectfully submits that these claims are allowable and patentable under 35 U.S.C. § 102.

Claims 3, 5 - 9 and 12, 14 - 17, 19 - 20 in this application are each dependent from one or the other of independent claims discussed above and are, therefore, believed allowable and patentable under 35 U.S.C. § 102 and 103 for the same reasons.

A review of the other art of record has failed to reveal anything which, in the applicants' opinion, would remedy the deficiencies of the art discussed above as referenced against the claims now present in this application. The claims are, therefore,

believed patentable over the art of record.

In view of the foregoing remarks, applicants respectfully request favorable reconsideration and early passage to issue of the present application.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to kindly telephone the undersigned at the telephone number listed below. If there are any fees due and owing, please charge Deposit Account No. 502-470.

Respectfully submitted,

Date: 4/28/03

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231 on 4/28/03.

Steve Cha, Reg. No. 44,069
(Name of Registered Representative)

4/28/03
(Signature and Date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Patent Application of

Inventor(s): Dong-Su Kim Group Art Unit: 2823

Serial No.: 09/899,784 Examiner: Toledo, Fernando L

Filing Date: July 5, 2001

For: Method of Fabricating Silica Microstructures

Assistant Commissioner for Patents
Washington, D.C. 20231

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please amend the specification as follows:

Page 1, in the paragraph beginning on line 5, change as follows:

This application claims priority to an application entitled "Method of Fabricating Silica Microstructures", filed in the Korean Intellectual~~dustrial~~ Property Office on July 6, 2000 and assigned Serial No. 2000-38692, the contents of which are hereby incorporated by reference.

IN THE CLAIMS

Please cancel claims 2, 11 and 18 without prejudice and amend the claims as follows: